What is claimed is:

1. An apparatus comprising:

a storage structure to store at least one entry, the at least one entry to include a register identifier value;

a first physical rename register of a first length; and

a second physical rename register of a second length different than the first length;

wherein the register identifier value is to indicate a current length, wherein the current length is selected from a set including the first length and the second length.

2. The apparatus of claim 1, wherein:

the first and second rename registers belong to a plurality of n physical rename registers, wherein $n > 2$;

each of the n physical rename registers is of a distinct length; and

the set includes each of the n distinct lengths.

3. The apparatus of claim 1, wherein:

the storage structure is to store a plurality of entries, each of the plurality of entries to include a corresponding register identifier value.

4. The apparatus of claim 1, wherein:

the first physical rename register is one of a plurality (z) of physical rename registers of the first length.

5. The apparatus of claim 1, wherein:

the second physical rename register is one of a plurality (m) of physical rename registers of the second length.

6. The apparatus of claim 4, wherein:

the second physical rename register is one of a plurality (m) of physical rename registers of the second length.

7. The apparatus of claim 6, wherein:

z is not equal to m.

8. The apparatus of claim 1, further comprising:

a logical register; and

rename logic to map an instance of the logical register to a selected physical rename register, where the selected physical rename register is selected from a plurality of registers comprising the first physical rename register and the second physical rename register.

9. The apparatus of claim 8, wherein:

the logical register includes a plurality of n bit positions;

a selected one of the n bit positions may be accessed individually responsive to a first instruction that indicates the selected bit position;

all n bit positions may be accessed together responsive to a second instruction; and

the rename logic is further to allocate the first physical rename register responsive to the first instruction, the rename logic further to allocate the second physical rename register responsive to the second instruction.

10. The apparatus of claim 9, wherein:

a subset including y of the n bits may be accessed responsive to a third instruction, where $y > 1$; and

the rename logic is further to allocate the first physical rename register responsive to the third instruction.

11. The apparatus of claim 10, wherein:

the length of the first physical rename register includes y bit positions.

12. The apparatus of claim 11, wherein:

the entry is further to include a position identifier, the position identifier to indicate a selected one of the y bit positions of the first physical rename register.

13. The apparatus of claim 12, wherein:

the selected one of the y bit positions of the first physical rename register corresponds to the selected bit position indicated by the first instruction.

14. A method comprising:

determining if a current instruction indicates a multiple-bit-field (MBF) register having n bit positions, where $n > 1$;

wherein the MBF register is to be written in accordance with any of a plurality of access types, the plurality of access types including:

a partial-bit write of 1 bit position;

a bulk-bit write of x bit positions, where $1 < x \leq n$;

allocating a physical rename register for the destination register;

wherein allocating further comprises allocating a physical rename register of a first length if the current instruction indicates a partial-bit write and further comprises allocating a physical rename register of a second length if the current instruction indicates a bulk-bit write.

15. The method of claim 14, wherein:

allocating further comprises modifying a rename map table to indicate the allocated physical rename register.

16. The method of claim 14, wherein:

the plurality of access types further includes a partial-bit write of y bit positions, where 1 < y < x.

17. The method of claim 14, wherein:

the y bit positions are contiguous.

18. The method of claim 14, wherein:

the x bit positions are contiguous.

19. The method of claim 14, wherein:

the plurality of access types includes a bulk-bit write of all n bit positions.

20. The method of claim 16, wherein:

y=2.

21. The method of claim 16, wherein:

y=4.

22. The method of claim 14, further comprising:

modifying the current instruction to indicate the allocated physical rename register in place of the MBF register.